PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2001-083208**
(43)Date of publication of application : **30.03.2001**

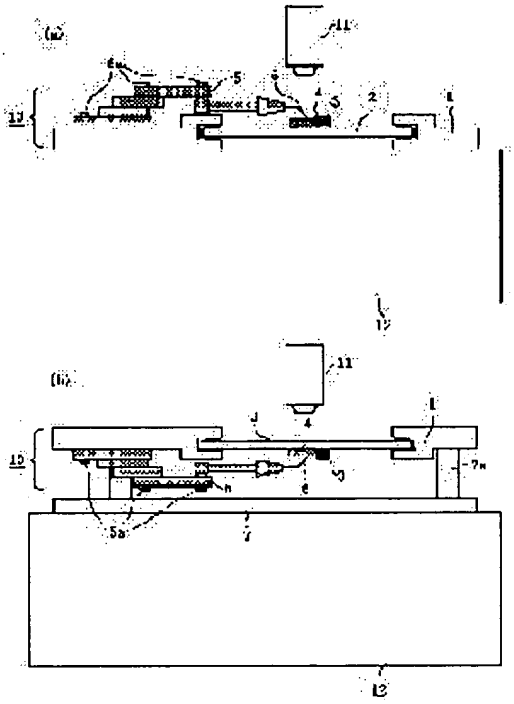
(51)Int.Cl. **G01R 31/26**
G01N 21/95

(21)Application number : **11-258328**
(22)Date of filing : **13.09.1999**

(71)Applicant : **NEC CORP**
(72)Inventor : **KITAHATA HIDEKI**

(54) PROBER FOR ANALYZING SEMICONDUCTOR CHIP AND SEMICONDUCTOR CHIP ANALYZER

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain both a front surface analysis and a rear surface analysis at a low cost in a short TAT in a semiconductor device evaluation analysis using a photodetection of a semiconductor chip.
SOLUTION: The analyzing prober 10 comprises a board 1 having a size equivalent to that of a semiconductor wafer, a quartz plate 2 provided in an opening of the board 1, and a manipulator 5 provided on the board 1. A semiconductor chip 4 is pressed on the plate 4 and fixed by utilizing a pressure of a probe 6 in the case of probing. When front surface analyzed, the prober 10 is mounted as shown in FIG. (a) on a wafer stage 12 of a normally used wafer analyzer, and analyzed by utilizing an optical system 11 while electrically inputting by the probe 6. When rear surface analyzed, a detachable plate 7 is mounted, the prober 10 is reversed back side front as shown in FIG. (b), mounted on the stage 12, and analyzed by utilizing the system 11 while electrically inputting by the probe 6.



LEGAL STATUS

[Date of request for examination]	08.08.2000
[Date of sending the examiner's decision of rejection]	08.08.2002
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3388462
[Date of registration]	17.01.2003
[Number of appeal against examiner's decision of rejection]	2002-17369
[Date of requesting appeal against examiner's decision of rejection]	09.09.2002
[Date of extinction of right]	

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] It is the prober for semiconductor chip analysis which it is the prober for semiconductor chip analysis equipped with the chip stage in which a semiconductor chip is carried, and two or more probes which contact this semiconductor chip from the front-face side of said semiconductor chip, and the part of said chip stage which contacts a semiconductor chip at least is constituted by the infrared transparency plate, and is characterized by for said semiconductor chip to be pushed on said chip stage by the pressure at the time of probing of said probe, and to be fixed it on said chip stage.
[Claim 2] Said probe is a prober for semiconductor chip analysis according to claim 1 characterized by the upper and lower sides and horizontal migration being possible with the manipulator supported by said chip stage.
[Claim 3] The prober for semiconductor chip analysis according to claim 1 or 2 characterized by forming the skid supporting at least 1 side face of a semiconductor chip on said chip stage.
[Claim 4] The prober for semiconductor chip analysis given in any of claims 1-3 to which an infrared transparency plate is characterized by being constituted with quartz glass they are.
[Claim 5] The prober for semiconductor chip analysis given in any of claims 1-4 characterized by containing the probe of a dummy without electrical installation to said semiconductor chip in said probe, and performing probing also by the probe of this dummy they are.
[Claim 6] The prober for semiconductor chip analysis given in any of claims 1-5 characterized by constituting said chip stage including the infrared transparency plate with which said semiconductor chip is carried, and the board which holds said infrared transparency plate and supports said manipulator they are.
[Claim 7] The prober for semiconductor chip analysis according to claim 6 to which the base of said infrared transparency plate is characterized by carrying out outline coincidence with the base of said board.
[Claim 8] Said infrared transparency plate is a prober for semiconductor chip analysis according to claim 6 or 7 characterized by being held airtightly at said board.
[Claim 9] The prober for semiconductor chip analysis given in any of claims 1-8 characterized by it being possible to install the removable sheathing which covers the upper part on said chip stage where probing is performed to said semiconductor chip they are.
[Claim 10] The prober for semiconductor chip analysis according to claim 9 characterized by preparing the stanchion for fixing said sheathing on said chip stage.
[Claim 11] The prober for semiconductor chip analysis indicated by any of claims 1-10 they are where probing is performed to said semiconductor chip On a prober stage, said semiconductor chip of said chip stage or said sheathing and the field which counters the field of the opposite side in the condition of having made it contacting on said prober stage Semiconductor chip analysis equipment characterized by the ability to perform analysis to said semiconductor chip using the optical system which carried and was installed in said prober stage upper part.
[Claim 12] Said prober stage is semiconductor chip analysis equipment according to claim 11 characterized by holding said prober for semiconductor chip analysis by carrying out vacuum suction of said chip stage or said sheathing.
[Claim 13] Semiconductor chip analysis equipment according to claim 11 or 12 characterized by using the wafer stage of the wafer analysis equipment which equipped said prober stage with the optical system for analyzing a wafer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the prober for semiconductor chip analysis and analysis equipment for evaluating especially a semiconductor chip optically about the prober for analysis and analysis equipment for analyzing a semiconductor chip.
[0002]
[Description of the Prior Art] EMS (Emission Microscope) which observes the light generated from a failure part etc. with photodetection equipment as an approach of performing evaluation and analysis of a semiconductor device while impressing an electrical potential difference to a semiconductor device -- OBIC (Optical Beam Induced Current) which detects law and current change which scans a semiconductor chip front face with laser light, and is generated in a failure part etc. -- there is law etc. Drawing 13 is the sectional view showing the conventional example of the wafer analysis equipment which performs evaluation and analysis of this kind of semiconductor device in the state of a wafer. The optical system 11 for analyses, such as a CCD camera and laser, is arranged up, a front face is turned upward and the semi-conductor wafer 13 is put on the wafer stage 12. It justifies by moving the wafer stage 12 so that an analyzed chip may come under the optical system 11 for analysis. And vacuum adsorption is carried out by the wafer stage 12 with the small porosity which can carry out vacuum adsorption, and the semi-conductor wafer 13 is fixed. Then, checking a wafer front face using the microscope 14 for probe localization from the upper part, the location of a probe (metal probe) 6 is set up by the following approaches of operation, and probing is performed. It is carried out when actuation of the direction of a semi-conductor wafer front face operates adjustment handle 24a of the manipulator 5 with which actuation of the vertical direction of a probe 6 was fixed to the platen 15 again using handle 24b for adjustment.
[0003] Thus, after probing is carried out, an electrical input is performed to the integrated circuit in a semiconductor chip through a probe 6, and the semiconductor chip front face by the detection and the laser beam of light which were generated from the failure part etc. using the optical system 11 for analysis is scanned from the upper part. The optical system 11 for analysis performs evaluation analysis of an analyzed chip to coincidence by observing the surface image of an analyzed chip together with observation of light, and pinpointing the generating part of light, and the generating part of current change etc. From ****, both optical detection and an optical scan, and probing will be performed from a chip front face in the usual analysis by probing. In addition, the microscope 14 for probe localization and the optical system 11 for analysis may be installed as a thing of one equipped with both functions.
[0004] however, the EMS method and OBIC which used the infrared light with high transmission to a semi-conductor as the failure analysis technique of such an integrated circuit by multilayer-interconnection-ization progressing with large-scale-izing of a semiconductor integrated circuit in recent years, and it becoming difficult to pinpoint a failure part from the chip front face covered with metal wiring -- the technique (the rear-face analysis technique) of detecting a defect part from a chip rear face is performed by law etc. However, if the rear-face analysis technique in which the light which can be used is limited to an infrared region has problems, like detection sensitivity is blunt compared with the analysis from the chip front face where a larger wavelength region is available and depends on a case, the surface analysis technique may become effective. From the need of coping with such a situation, many equipments in which both a chip front face and a rear face to evaluation and analysis are possible are marketed. In such analysis equipment, after performing an electrical input from the front face of a semiconductor chip in which the integrated circuit is formed, it is necessary to hold a semiconductor chip from a chip rear face according to the gestalt which can perform optical observation from a chip front face at the time of surface analysis at the time of rear-face analysis. For the reason, in such analysis equipment, the expensive optical system for analysis which bears the detection function of a fault is fixed to one line, and, generally, the technique of making the front flesh side of a semiconductor chip reverse, and holding it by the case of surface analysis and rear-face analysis, is adopted.
[0005] For example, to the rear-face analysis technique, a chip rear-face side can be responded to any analysis technique comparatively easily by opening a chip front-face side to the surface analysis technique by mounting a semiconductor chip in a mold package with comparatively easy processing etc. That is, even if it makes the front flesh side of the whole package reverse and holds it, since the input/output terminal of an integrated circuit is pulled out by the lead terminal of the package circumference, an electrical input becomes possible through a lead terminal. However, there is a problem that Analysis TAT (turn around time) becomes long, for the time amount concerning mounting and opening to a package. Drawing 14 is the sectional view

of the mold package in which the rear-face analysis technique is shown. After mounting a semiconductor chip 4 on an island 16, wirebonding is performed, lead 17 is connected with the input/output terminal of an integrated circuit, and a semiconductor chip 4 and a bonding wire 18 are further fixed with mold resin 19. Then, the mold resin 19 and the island 16 on the rear face of a chip are removed, and the rear-face opening 20 to which a chip rear face is exposed is established. And in the analysis equipment which has a package chassis box, after performing electric I/O from lead 17, rear-face analysis is performed through the rear-face opening 20.

[0006] Since the direction of probing will also become reverse on the other hand if the front flesh side of a chip is made reverse in analyzing [which needs probing] to an electrical input with the chip which is not mounted in a package, or a wafer condition, this modification is not easy. Drawing 15 is the sectional view showing the condition of performing probing from the bottom for the rear-face analysis of the analysis equipment which optical system 11 has been arranged up, and was constituted so that probing might be more possible than a top and down one to a semi-conductor wafer. In this case, the semi-conductor wafer 13 is put on the opening 22 for analysis established in the center section of the attachment-and-detachment type wafer stage 21 so that an analyzed chip may come, and it is made to fix to it by vacuum adsorption using the a large number hole prepared in the contact surface by the side of the attachment-and-detachment type wafer stage 21. Then, probing is performed by operating the adjustment handles 24a and 24b of the manipulator 5 installed in the platen 15 like the aforementioned conventional example, checking [set the attachment-and-detachment type wafer stage 21 so that a chip rear face may turn / applied part / (with no illustration) / with which analysis equipment was equipped / wafer stage / to the upper part, and] a wafer front face with CCD camera 23 for probe localization from a lower part. And after performing an electrical input to the integrated circuit in a semiconductor chip through a probe 6, rear-face analysis is performed using the optical system 11 for analysis from the above-mentioned opening 22. In addition, after removing the attachment-and-detachment type wafer stage 21 and CCD camera 23, placing the wafer stage for surface analysis caudad and fixing a semi-conductor wafer on it while attaching a manipulator 5 in the opposite side of a platen 15 in performing surface analysis using this analysis equipment, the optical system 11 for analysis united with the microscope performs probing and surface analysis from the upper part.

[0007]

[Problem(s) to be Solved by the Invention] Analysis TAT becomes long especially in my hearing that Analysis TAT becomes long and there being the 1st trouble, when a semiconductor chip is mounted in a package and it analyzes it, and performing rear-face analysis. The reason is because it is necessary to open a desired part for failure analysis after mounting a semiconductor chip in a package, in order to make possible the electrical input to a semiconductor integrated circuit. After fixing a chip rear face by the brazing filler metal on an island at the time of surface analysis, although analysis becomes possible also by simple mounting of only performing bonding, since it is difficult to perform bonding, opening a chip rear face wide, it is difficult in the case of rear-face analysis to cope with it by simple mounting. In this case, after fixing a chip rear face by the brazing filler metal on an island and performing wirebonding, it is necessary to fix a semiconductor chip, a bonding wire, and a lead with mold resin etc., and to perform removal of the mold resin by the side of a chip rear face, an island, and a brazing filler metal, and mirror polishing on the rear face of a semiconductor chip further.

[0008] The 2nd trouble is in the condition which carried out probing to the semiconductor chip, and when it also enables analysis from which direction of a chip front face and a chip rear face, it is that analysis cost becomes high. The analysis equipment with which the reason reconciled surface analysis and rear-face analysis is because it becomes expensive. The optical system for analysis which bears the detection function of a fault is fixed to one line, and since the direction of probing also becomes reverse when making the front flesh side of a semiconductor chip reverse and holding it in surface analysis and rear-face analysis, the expensive prober equipped with the special probing device is needed. On the other hand, if the optical system for analysis which bears the detection function of a fault is extended to two lines, after fixing the direction of probing to one side, surface analysis and rear-face analysis will be attained. However, the need of exposing to coincidence the chip rear face which performs detection optical for rear-face analysis, and the chip front face which performs probing does not change, but by the addition of the expensive optical system for analysis, analysis equipment will become still more expensive rather than it adds a special probing device.

[0009] Since the configuration of a semiconductor chip will be restrained if it is going to fix a semiconductor chip to a stage by vacuum adsorption when turning a semiconductor chip rear face up and carrying out probing from a lower part, the 3rd trouble is that the semiconductor chip analysis of a specific configuration becomes difficult. In the case of the chip of a dimension configuration smaller than stage opening for rear-face analysis, the reason is because the maintenance field for vacuum adsorption is not securable for a chip periphery. If stage opening is too large, a small chip is unfixable, and if stage opening is too small, observation of the whole chip will become difficult. When analysis cost will be pulled up, preparing many stages equipped with the vacuum adsorption device, although maintenance of the semiconductor chip of various configuration and dimensions will be attained on the other hand if many stages where the magnitude of opening differs are prepared also becomes causing protraction of Analysis TAT, if the stage is created for every analysis. Moreover, since the maintenance field for vacuum adsorption is covered with a stage and rear-face analysis cannot be performed, the defect of the field also has the problem of being undetectable. Therefore, in the fixed approach by vacuum adsorption, analyzing the whole semiconductor chip cut down by the pellet type is that it is difficult.

[0010] The 4th trouble is that there is a difficulty in the workability, when a semiconductor chip rear face is turned up and carries out probing from a lower part. The reason is for having to perform observation on the front face of a semiconductor chip within the visual field to which it was restricted [CCD camera]. Making it move to the bottom of a microscope, and checking the

location of the pad on a probe and a semiconductor chip (electric terminal section) under a microscope, after checking the location in a wafer of an analyzed chip by viewing at the time of a setup of the usual wafer prober which analyzes by turning a semiconductor chip front face up, a manipulator is operated and probing is performed. If a microscope observation image is an erect normal image at this time, since the direction of the probe observed in the microscopic field and the direction of the manipulator to operate are in agreement, workability is good. However, since it becomes the posture which looks up at a top from the bottom in viewing when observing a semiconductor chip front face, where a semiconductor chip rear face is turned up, the workability of probing worsens.

[0011] Then, although the monitor image by a CCD camera etc. is used like the above-mentioned conventional example in many cases, in the visual field restricted [CCD camera], the workability at the time of doing the activity which selects a specific analyzed chip from on the wafer with which much chips of the same pattern were located in a line worsens. Moreover, when operating a manipulator, by the time the direction of the probe observed on a screen and the direction of the manipulator to operate come to be sensuously in agreement, looking at a monitor image, some skill nature will be needed. Although it is also possible to use the electromotive manipulator and electromotive stage which can be operated by remote control, and to operate probing on the monitor of a computer in order to improve these workability, so much, an analysis facility also becomes expensive and there is a problem that analysis cost goes up.

[0012] after [therefore,] performing probing to a semiconductor chip using the analysis equipment which has the wafer stage for wafer probers which the technical problem of this invention is solving the trouble of the conventional technique mentioned above, and the purpose turns a wafer front face up, and is fixed -- from any direction of a chip front face and a chip rear face -- analysis -- possible -- carrying out -- low cost -- and -- short -- it is making TAT failure analysis possible.

[0013]

[Means for Solving the Problem] The chip stage in which a semiconductor chip is carried according to this invention in order to attain the above-mentioned purpose, Two or more probes which contact this semiconductor chip from the front-face side of said semiconductor chip, Are a prober for preparation ********** analysis and the part of said chip stage which contacts a semiconductor chip at least is constituted by the infrared transparency plate. And prober ** for semiconductor chip analysis characterized by for said semiconductor chip being pushed on said chip stage by the pressure at the time of probing of said probe, and fixing it on said chip stage is offered.

[0014] And the upper and lower sides and horizontal migration are possible for said probe by the manipulator supported by said chip stage preferably. Moreover, the skid supporting at least 1 side face of a semiconductor chip is preferably formed on said stage. Furthermore, preferably, it is in the condition which performed probing to said semiconductor chip on said chip stage, and it is possible to install the removable sheathing which covers the upper part.

[0015] In order to attain the above-mentioned purpose, where probing is performed to said semiconductor chip, according to this invention, moreover, the above-mentioned prober for semiconductor chip analysis On a prober stage, said semiconductor chip of said chip stage or said sheathing and the field which counters the field of the opposite side in the condition of having made it contacting on said prober stage It carries and semiconductor chip analysis equipment ** characterized by the ability to perform analysis to said semiconductor chip using the optical system installed in said prober stage upper part is offered.

[0016] And said prober stage holds said prober for semiconductor chip analysis preferably by carrying out vacuum suction of said chip stage or said sheathing. Furthermore, said prober stage upper part is equipped with optical system, and at least one side of said prober stage and said optical system is horizontally movable to it.

[0017]

[Function] The prober for analysis of this invention has the description of becoming possible to fix a semiconductor chip with the pressure of probing, by forming the skid the top which can be miniaturized in order to perform probing in the state of the semiconductor chip cut down from the semi-conductor wafer. Therefore, when the effectiveness that the device of vacuum adsorption becomes unnecessary and immobilization of the chip of more various configurations is attained is acquired, since structure is small and simple, a manufacturing cost is also held down low. Moreover, it carries, carrying out probing by miniaturization, since lightweight-izing is also possible, or the handling of making a front flesh side reverse etc. becomes easy. That is, the same effectiveness as performing failure analysis upwards and mounting in a package only by probing will be acquired, and since the time amount mounted in a package is omissible, compaction of Analysis TAT is attained.

[0018] Moreover, since the prober for analysis of this invention forces the rear face of a semiconductor chip on the plate which can penetrate infrared light and fixes to it, it has the description which can perform rear-face analysis through an infrared transparency plate. Therefore, compared with the case where mount in a package and rear-face analysis is performed, the activity which opens a chip rear face becomes unnecessary, and the effectiveness that Analysis TAT is shortened further is acquired. Since the maintenance field for vacuum adsorption is not needed for a chip periphery compared with the case where fix a semiconductor chip by vacuum adsorption and probing is performed on the other hand, the effectiveness that the analysis on the whole rear face of a semiconductor chip of more various configurations is attained is acquired. Furthermore, even if the prober for analysis of this invention reverses a front flesh side by having the device in which it equips with a removable plate, it can be fixed by vacuum adsorption on the wafer stage for the wafer probers used for the surface analysis technique which turns a wafer front face up and is fixed. Therefore, with the analysis equipment which has the wafer stage for wafer probers used for the usual surface analysis technique, since the analysis of both surface analysis and rear-face analysis is attained, expensive analysis equipment becomes unnecessary and the effectiveness that the rise of analysis cost can be suppressed can be acquired.

[0019]

[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained to a detail with reference to a drawing.
[The gestalt of the 1st operation]
[Explanation of a configuration] Drawing of longitudinal section of the prober for analysis for [in / in drawing 1 / this invention] explaining the gestalt of the 1st operation and drawing 2 are the perspective view. The whole frame consists of boards 1 on which the prober 10 for semiconductor chip analysis of this invention has the dimension of semi-conductor wafer extent, and some or all of the board 1 is constituted by the quality of the material which can penetrate infrared light like the quartz plate 2. The convex skid 3 for two or more manipulators 5 for performing probing upwards on the basis of the board 1 being arranged, and supporting at least 1 side face of a semiconductor chip 4 in the field which can penetrate the infrared light on the board is arranged. In addition, the skid 3 is formed of what it is [glass / plastics,] easy to process. Furthermore, on the board 1, it has the wrap removable plate 7 and stanchion 7a for supporting it in the board upper part (in drawing 2 , the removable plate 7 and stanchion 7a are not shown). In addition, the removable plate 7 is attached in a board 1 on a screw etc. if needed (at namely, the time of rear-face analysis). Although stanchion 7a is being fixed to the removable plate 7 side, it fixes to the board side and you may make it a stanchion detach and attach a removable plate to the stanchion with the gestalt of this operation.
[0020] In addition, although the board 1 has structure which puts the quartz plate 2 between the metal plates of two sheets in drawing 1 , this is for maintaining mechanical reinforcement by constituting with a metal the part which arranges a manipulator 5 and stanchion 7a. Furthermore, in case a board 1 is made to fix by vacuum adsorption on the wafer stage of a wafer prober at the time of surface analysis, board 1 base is evenly ground by extent which can be stuck and placed on a wafer stage, and it is good between a metal plate and the quartz plate 2 to make it make it stick through the O ring made of rubber etc. Moreover, in order to perform rear-face analysis, the part of the board 1 which contacts semiconductor chip 4 rear face at least, and is fixed must be constituted by the ingredient which can penetrate infrared light. In addition, the removable plate 7 is a thing for fixing by vacuum adsorption, when placing the prober for analysis of this invention on the wafer stage for the usual wafer probers used for the surface analysis technique and performing rear-face analysis. Therefore, as for the top face, it is desirable to be evenly ground by extent which can be stuck and placed on a wafer stage.
[0021] By the small prober, a manipulator 5 equips the thing of the smallest possible dimension configuration in order to make more probing possible. For example, since a dimension becomes large, the manipulator of form to which the adjustment handles 24a and 24b for turning the screw which justifies a probe as shown in drawing 15 were attached has the thing of form in which a screw is turned for stretching screw 5a as shown in drawing 1 using a fixture like a driver, and the desirable thing of form with a removable handle part. When placing the prober for analysis of this invention on the wafer stage for the usual wafer probers and performing rear-face analysis especially, the problem that the fixed position of a semiconductor chip becomes higher than the location of the usual semi-conductor wafer arises. Also in this case, in order to enable rear-face analysis by the wafer stage for the usual wafer probers, it must avoid that the fixed position of a semiconductor chip becomes high more than the movable range of the optical system for analysis. If the manipulator 5 of the low mold of ** which can stop low the height of stanchion 7a as shown in drawing 1 for the reason is used, it will become possible to fill such a demand.
[0022] It can be made to fix by vacuum adsorption in the prober for analysis of this invention which consists of the above-mentioned configuration on the wafer stage of the analysis equipment which has the usual wafer prober in the case of surface analysis or rear-face analysis. A thing with highly precise stage migration capacity is in usual wafer analysis equipment so that a coordinate can be set up and used for pinpointing of the defect part in a semiconductor chip on a wafer stage. However the migration precision of a wafer stage may be excellent, if the semiconductor chip on a stage is not fully being fixed, since a fixed position shifts delicately by vibration in the case of stage migration etc., it becomes impossible however, to specify the coordinate of a fault correctly. Therefore, when using the coordinate of a wafer stage for pinpointing of the defect part in analysis, immobilization by vacuum adsorption is indispensable.
[0023] [Explanation of operation] In advance of implementation of evaluation analysis, first the base of the semiconductor chip 4 which analyzes on a board 1 It changes into the condition at the time of assigning and carrying out probing of the probe 6 to the pad on a semiconductor chip with a skid 3 and the manipulator 5 arranged in the location of the opposite side a core [a semiconductor chip 4], after assigning a side face to a skid 3. As shown in drawing 3 (a), it fixes by vacuum adsorption on the wafer stage 12 of usual wafer analysis equipment. And the microscope outside drawing with which wafer analysis equipment is equipped standardly is used, stretching screw 5a of a manipulator 5 is adjusted, and probing is performed. Thereby, a semiconductor chip 4 is pushed and fixed in the direction of a base, and the direction of a side face by the force from a probe 6. In addition, the probing device with which this analysis equipment is equipped from origin is removed at this time. Or it shunts in the location which does not compete with the prober 10 for this semiconductor chip analysis.
[0024] Then, when performing evaluation and analysis by the approach of surface analysis, with this condition, an electrical input is performed through a probe 6 and evaluation and analysis of a semiconductor chip 4 are performed from the front-face side of a semiconductor chip 4 using optical system 11. After removing the prober 10 for analysis from the wafer stage 12, as it equips with the removable plate 7 on a board and is shown in drawing 3 (b), the prober 10 whole for analysis is turned inside-out, and the removable plate 7 is turned down, and in carrying out by the approach of rear-face analysis, on the wafer stage 12, vacuum suction is laid and carried out and it fixes. After setting it as such a condition, an electrical input is performed through the probe 6 of the prober for analysis, and the defect part is detected from the rear-face side of a semiconductor chip 4 through the quartz plate 2. In addition, if the prober for analysis needs to be justified, it will adjust by moving the wafer stage 12.
[0025] Next, the relation of the force applied to a semiconductor chip with reference to drawing 4 at the time of probing is explained. When the location of a manipulator and a skid 3 performs probing to a semiconductor chip 4, it is beforehand arranged

in a location where a semiconductor chip 4 is pushed against a skid 3 by the pressure. Probing to a semiconductor chip 4 presses the point of the probe 6 which gave the inclination to the direction of a normal of a chip side to the pad on a semiconductor chip, and performs it. Probe ** which a semiconductor chip 4 receives from a probe 6 at this time consists of probe ** 8v which it is going to force caudad, and 8h of probe ** which it is going to let slide horizontally with the elasticity of a probe 6, as shown in drawing 4 . Among these, when repulsive force 9v which receives the former from the quartz plate 2, and the latter balance with 9h of repulsive force received from a skid 3, a semiconductor chip 4 is fixed. A skid 3 may be easily fixed by thing like a removable double-sided tape so that it can respond to various chip configurations by adhesives 3a, although it fixes on the quartz plate 2. In addition, since it is small as compared with probe **, the gravity which joins a semiconductor chip 4 shall be disregarded here.

[0026] Then, the configuration of a skid required in order to make the semiconductor chip fix is explained. Drawing 5 - drawing 7 are the top views showing the example of the flat-surface configuration of a skid 3 respectively. The skid 3 of drawing 5 is effective, when only one side of a semiconductor chip 4 is supported and probe ** is concentrating on one of them. Although the direction of probing ** 9 does not necessarily restrict concentrating on an one direction, it is possible for adjusting the direction of probe ** as the whole by dummy probing which carries out probing of the suitable location in a chip with the probe 6 which does not perform electrical installation. There are few probing need terminals, and such dummy probing is effective also when probe ** required to fix a semiconductor chip 4 also including the time of back ** of the prober for analysis at the time of rear-face analysis run short.

[0027] However, if it depends on the number of probing need terminals, an available probe may not be securable for dummy probing for adjusting the direction of probe **. In that case, as shown in drawing 6 and drawing 7 , by supporting two sides, it is stabilized and a semiconductor chip 4 can be fixed. what supports the skid 3 of drawing 6 centering on one corner of a semiconductor chip 4 -- it is -- probe ** -- the corner -- it is more effective, if it arranges so that it may concentrate near. Although drawing 7 also supports two sides of a semiconductor chip 4, since the angle which each skid 3 constitutes can be adjusted even when the angle of two sides to accomplish has separated from the right angle depending on how to cut down a semiconductor chip 4 etc., since he is trying to support each side with the separate skid 3, it is possible for it to be stabilized more and to fix. Furthermore, since he is trying to support two points of semiconductor chip 4 edge, by adjusting the sense of a semiconductor chip 4 so that keeping with probing ** 9 can be taken, also in the chip of more various configurations, such as a broken piece of ** of a wafer, the skid 3 of drawing 8 is stabilized and can be fixed.

[0028] [Gestalt of the 2nd operation] Drawing of longitudinal section of the prober for analysis for drawing 9 to explain the gestalt of operation of the 2nd of this invention and drawing 10 are the perspective view. Although probing by the manipulator generally has the advantage that it can respond flexibly also to the semiconductor chip with which a dimension configuration differs from pad arrangement, since the occupancy area on the board per manipulator is large, a probing possible number will be restricted by the area of a board. As shown in drawing 1 and drawing 2 , in the gestalt of the 1st operation, the manipulator 5 is arranged centering on the semiconductor chip 4 only in the location of a skid 3 and the opposite side. On the other hand, when it can have allowances in the area of a board, it is good to make it the gestalt of the 2nd operation as shown in drawing 9 and drawing 10 . In addition to manipulator 5A of the location of a skid 3 and the opposite side, as the structure, manipulator 5B is arranged centering on the semiconductor chip 4 also at the same side as a skid 3. About other structures, it is the same as that of the gestalt of the 1st operation. Moreover, detection of a fault, the approach of analysis, etc. are performed like the gestalt of the 1st operation. Therefore, it becomes possible about further much probing by using the equipment of the gestalt of this operation.

[0029] Next, the relation of the force applied to a semiconductor chip at the time of probing is explained. Although the horizontal force generated by probe ** by manipulator 5B arranged at the same side as a skid 3 will commit a semiconductor chip 4 in the direction pulled apart from a skid 3, unless it becomes larger than the horizontal force generated by probe ** by manipulator 5A arranged in a skid 3 and the opposite side, it is possible for putting a pressure which pushes a semiconductor chip 4 against a skid 3 as a whole. That is, first, the base of a semiconductor chip 4 and a side face are forced by probing by manipulator 5A arranged in a skid 3 and the opposite side, and a semiconductor chip 4 is fixed, after the base was assigned by the board 1 and a side face is assigned to it by the skid 3. Then, probing becomes possible, without shifting the fixed position of a semiconductor chip 4 by carrying out probing by manipulator 5B arranged at the same side as a skid 3. The horizontal force generated by probe ** by manipulator 5B arranged temporarily at the same side as a skid 3 at this time Become larger than the horizontal force generated by probe ** by manipulator 5A arranged in a skid 3 and the opposite side, and as a whole, even if the force of the direction which pulls apart a semiconductor chip 4 from a skid 3 works Unless the force turns into bigger force than the frictional force committed between a semiconductor chip 4 and the quartz plate 2, the location of a semiconductor chip 4 does not shift.

[0030] Like drawing 10 , if the probing number is made to increase, the force which pushes a semiconductor chip 4 against the quartz plate 2 is large, and the repulsive force committed from the quartz plate 2 to a semiconductor chip 4 is also large. Therefore, as long as there are many extent with the same number of manipulator 5B arranged at the same side as a skid 3 and manipulator 5A arranged in a skid 3 and the opposite side or manipulator 5A, it is possible by carrying out probing in the above-mentioned procedure to fix a semiconductor chip 4 in the state of probing. Furthermore, like the gestalt of the 1st operation, by dummy probing, the direction of probe ** as the whole may be adjusted, or a semiconductor chip 4 may be fixed.

[0031] [Gestalt of the 3rd and operation of four] Drawing 11 and drawing 12 are drawings of longitudinal section showing the 3rd of this invention, and the gestalt of the 4th operation, respectively. With the gestalt of the 1st and the 2nd operation, when a board 1 is turned down and the prober 10 for analysis is carried on a wafer stage, there is a possibility of bending so that the quartz plate 2 may become convex by vacuum suction of a wafer stage. The gestalt of the 3rd and the 4th operation copes with

this point. He constitutes the quartz plate 2 from a gestalt of the 3rd operation in the configuration which is shown in drawing 11 and which has a height downward, and is trying for the base of the quartz plate 2 to be in agreement with the base of a board 1. There are no gestalt of the 1st operation and changing place which are shown in drawing 1 except this.

[0032] The appearance of the quartz plate 2 is made the same as the appearance of a board 1, and he prepares a height in the center section, and is trying to carry a semiconductor chip 4 there with the gestalt of the 4th operation shown in drawing 12 . The quartz plate 2 has fixed on the board 1 using adhesives etc. There are no gestalt of the 1st operation and changing place which are shown in drawing 1 except this. In addition, the gestalt of this 4th operation is changed and you may make it carry a semiconductor chip 4 on a flat quartz plate, without preparing a height in the quartz plate 2.

[0033] Although the gestalt of desirable operation was explained above, proper modification is possible for this invention within limits which are not limited to these and indicated by the claim. For example, although the prober for analysis concerning this invention was explained as what is carried on the wafer stage of wafer analysis equipment, it is not necessary to necessarily make it such, it prepares the analysis equipment of dedication, and you may make it this used for it with the gestalt of the above-mentioned operation. Also in this case, as for the stage where it is equipped with the prober for analysis of this invention, it is desirable that it is what can move with a relatively sufficient precision horizontally to optical system. Moreover, when preparing the analysis equipment of dedication, the pore for vacuum suction prepared in the stage in which the prober for analysis of this invention is laid is good only also as a part in contact with a board 1.

[0034]

[Effect of the Invention] As explained above, according to this invention, compaction of Analysis TAT is attained compared with the case where mount in a package and it analyzes as the 1st effectiveness. Since the first reason was carried or made easy the handling of making a front flesh side reverse etc., enabling small and lightweight-ization and carrying out probing as a prober for analysis by having been made to perform probing in the state of the semiconductor chip cut down from the semi-conductor wafer, it is a sake. That is, it is because the time amount which the same effectiveness as performing failure analysis upwards and mounting only probing in a package will be acquired, and is mounted in a package can be omitted. The second reason is that the activity which it becomes possible to perform rear-face analysis through a stage, and opens the mounted chip rear face becomes unnecessary by forcing the rear face of a semiconductor chip on the stage of the quality of the material which can penetrate infrared light, and fixing to it.

[0035] As the 2nd effectiveness, when analyzing by probing, it becomes possible to suppress the rise of analysis cost, enabling analysis of both surface analysis and rear-face analysis. The first reason is that a manufacturing cost is low held down since the device of vacuum adsorption of dedication becomes unnecessary and structure can do it small and simply by performing probing in the state of the semiconductor chip cut down from the semi-conductor wafer, and having fixed the semiconductor chip with the pressure of the probing. The second reason is that a front flesh side is only reversed, it becomes analyzable [both surface analysis and rear-face analysis], and expensive analysis equipment becomes unnecessary on the wafer stage for the usual wafer analysis equipments since the device in which it equipped with a removable plate was established after forcing the rear face of a semiconductor chip on the stage of the quality of the material which can penetrate infrared light and making it fix to it.

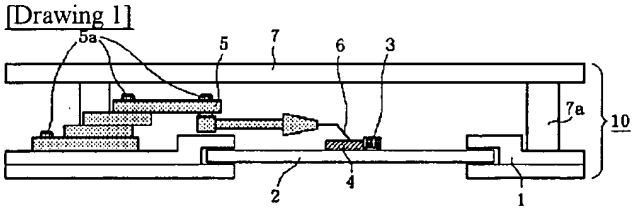
[0036] Compared with the case where fix a semiconductor chip by vacuum adsorption and rear-face analysis is performed as the 3rd effectiveness, it becomes possible to ease the constraint to the dimension configuration of a chip. The reason is that the maintenance field for vacuum adsorption is not needed for a chip periphery, but immobilization of the chip of more various configurations is attained by forcing the rear face of a semiconductor chip on the stage of the quality of the material which can penetrate infrared light, and fixing to it.

[Translation done.]

* NOTICES *

DRAWINGS

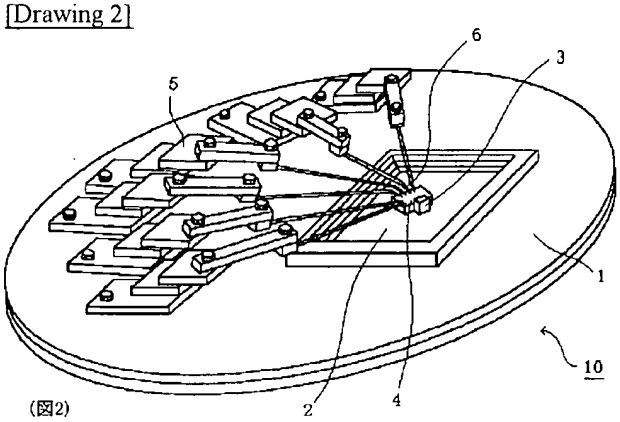
[Drawing 1]



(図1)

1 ボード　5 マニピュレータ
2 石英板　5a 調整ネジ
3 滑り止め　6 プローブ　7a 支柱
4 半導体チップ　7 着脱可能板　10 半導体チップ解析用プローバ

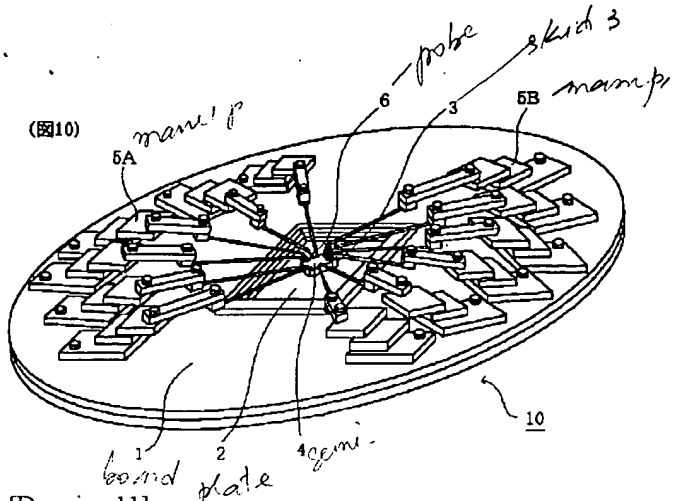
[Drawing 2]



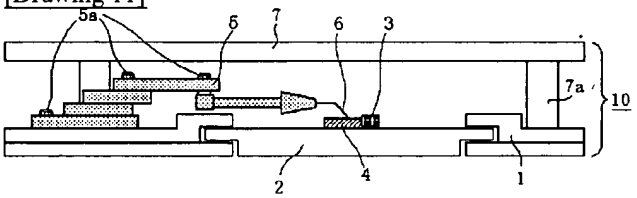
(図2)

[Drawing 3]

(図10)

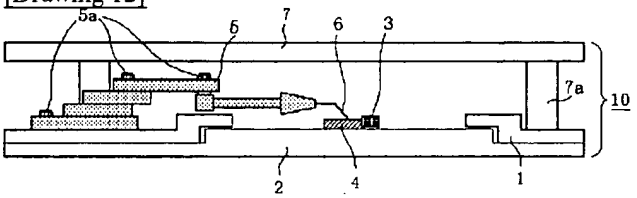


[Drawing 11]



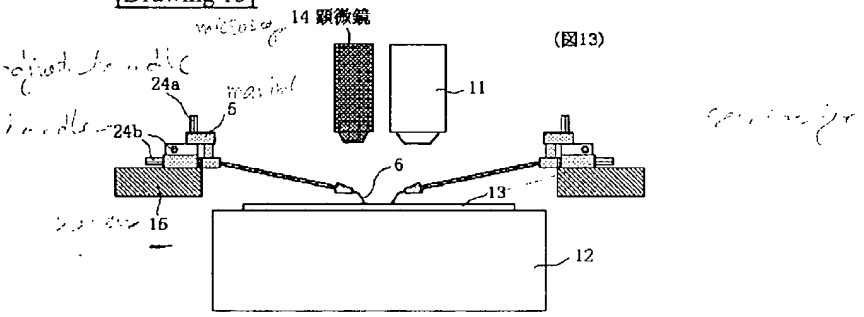
(図11)

[Drawing 12]



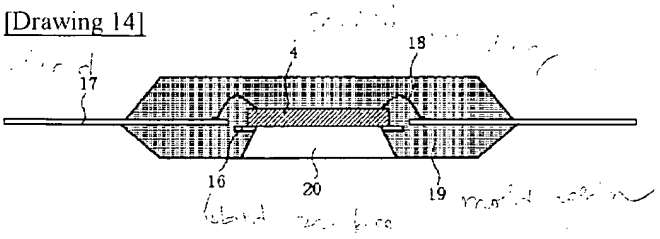
(図12)

[Drawing 13]



(図13)

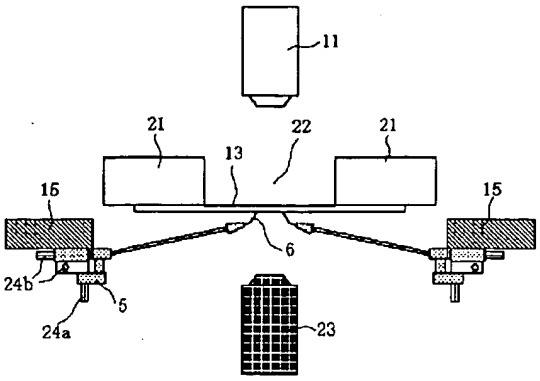
[Drawing 14]



16 アイランド
17 リード
18 ボンディングワイヤ
19 モールド樹脂
20 裏面開口部

(図14)

[Drawing 15]



13 半導体ウェハ
15 プラテン
21 着脱式ウェハステージ
22 開口部
23 CCDカメラ
24a、25b 調整ハンドル

(図15)

[Translation done.]